

semiconductor element in reverse parallel, a control circuit for generating and applying a gate voltage of the semiconductor element and the like.

Explanation of Designation

[0155] 10 source pad,
 [0156] 11 gate pad,
 [0157] 12 gate wiring,
 [0158] 13 drain electrode,
 [0159] 20 semiconductor substrate,
 [0160] 21 drift layer,
 [0161] 30 gate insulating film,
 [0162] 31 field insulating film,
 [0163] 32 interlayer insulating film,
 [0164] 33 gate insulating film and field insulating film boundary,
 [0165] 40 JTE region,
 [0166] 41 first well region,
 [0167] 42, 43 second well region,
 [0168] 45 high impurity concentration well region,
 [0169] 46, 47, 48 well contact region,
 [0170] 50 gate electrode,
 [0171] 61 source contact hole,
 [0172] 62 first well contact hole,
 [0173] 63 second well contact hole,
 [0174] 64 gate contact hole,
 [0175] 71 ohmic electrode,
 [0176] 72 back ohmic electrode,
 [0177] 80 source region,
 [0178] 81 field stopper region,
 [0179] 100 simplified element,
 [0180] 101 n-type semiconductor substrate,
 [0181] 102 n-type layer,
 [0182] 103 p-type well region,
 [0183] 104 p-type well contact,
 [0184] 105 interlayer insulating film,
 [0185] 106 upper electrode,
 [0186] 107 contact hole,
 [0187] 108 back electrode,
 [0188] 109 back ohmic electrode,
 [0189] 110 ohmic electrode,
 [0190] 111 gate insulating film,
 [0191] 112 gate electrode,
 [0192] 113 gate upper electrode.

1-9. (canceled)

10: A power semiconductor device comprising:

a semiconductor substrate of a first conductivity type or a second conductivity type;

a drift layer of the first conductivity type which is formed on a first main surface side of said semiconductor substrate;

a cell region formed in a part of a surface layer of said drift layer and constituted by a plurality of unit cells;

a second well region of the second conductivity type which is formed apart from said cell region on the periphery of said cell region;

a gate insulating film formed on said cell region and at said cell region side on said second well region;

a field insulating film formed on an opposite side to said cell region side on said second well region and having a greater film thickness than said gate insulating film;

a gate electrode formed on said gate insulating film and said field insulating film;

an interlayer insulating film formed on said gate electrode, said gate insulating film and said field insulating film;

a source contact hole formed to penetrate said gate insulating film and said interlayer insulating film on said cell region;

a second well contact hole formed to penetrate said field insulating film and said interlayer insulating film on said second well region;

a source pad for electrically connecting said cell region and said second well region through said source contact hole and said second well contact hole; and

a drain electrode formed on a second main surface side which is opposite to said first main surface.

11: The power semiconductor device according to claim 10, wherein a projection length from said second well contact hole of said second well region toward said cell region side is equal to or smaller than 100 μm .

12: The power semiconductor device according to claim 10, further comprising a first well contact hole formed to penetrate said gate insulating film on said second well region, said source pad electrically connecting said cell region and said second well region through said source contact hole, and said first well contact hole and said second well contact hole.

13: The power semiconductor device according to claim 10, further comprising:

a gate contact hole formed on said second well region; and a gate pad connected electrically to said gate electrode through said gate contact hole, wherein

said second well contact hole is formed on said cell region side from said gate contact hole.

14: The power semiconductor device according to claim 10, wherein said second well contact holes are formed to surround said cell region.

15: The power semiconductor device according to claim 10, wherein said semiconductor substrate and said drift layer are formed by a wide band gap semiconductor material.

16: The power semiconductor device according to claim 15, wherein said wide band gap semiconductor material is silicon carbide.

17: The power semiconductor device according to claim 10, wherein said second well region is a part of a surface layer of said second well region, and includes a high impurity concentration well region having a higher impurity concentration of the second conductivity type than other regions in said second well region under said second well contact hole.

18: The power semiconductor device according to claim 17, wherein said high impurity concentration well region is continuously formed under said gate electrode from a lower part of said second well contact hole.

19: The power semiconductor device according to claim 17, wherein said high impurity concentration well region is not formed under said gate insulating film provided on said second well region.

20: The power semiconductor device according to claim 10, wherein said unit cell includes a source region of the first conductivity type and a first well region of the second conductivity type, and

a channel region formed in said first well region interposed between said source region and said drift layer is parallel with said first main surface.